Application note: AsteRx-m3 / i3 Ethernet PHY

version 3.0

Feb 13, 2024

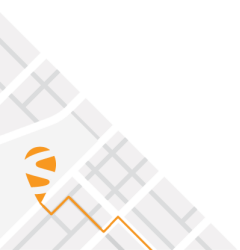

Table of Contents

Document Change Log

Version	Date	Affected	Change
1.0	20211008	All	Creation
2.0	20220728	All	Updating supported PHYs
3.0	20240213	All	Updating supported PHYs

1 Introduction

This document describes which ethernet PHY's are supported by the AsteRx-m3 and AsteRx-i3 receivers and which steps are needed to connect them.

The AsteRx-m3 and AsteRx-i3 receivers support full duplex 10/100 Base-T Ethernet communication. The Ethernet PHY and magnetics are to be implemented on the host board. Connection with the PHY is through the RMII interface available on the 60-pin connector.

The Hardware Manual provides an application circuit using the KSZ8041NL(I) PHY from Microchip, but other PHY's can be used.

2 Requirements

When selecting the external PHY, the following rules should be followed:

- The interface is RMII, if applicable the PHY needs to be configured by config pin strapping to use RMII.
- The AsteRx-m3 and AsteRx-i3 receivers will not reconfigure the PHY through PHY registers, the PHY can only be used in its default configuration or in a configuration that can be set with pin strapping.
- The RMII REF_CLK is 50 MHz
- By default, the Receiver (MAC) will not generate the 50 MHz REF_CLK and expects an RMII clock from the PHY, unless if it detects a KSZ8041NL(I) PHY. If the receiver detects a KSZ8041NL(I), it will generate the RMII clock itself.

  It is however possible to use a non-KSZ8041NL(I) PHY which expects a clock from the MAC. This can be done by upgrading the receiver with the **rmiiclk_from_mac.suf** file found in the **Ethernet PHYs** folder of the firmware package. This persistently enables the REF_CLK, overruling the default behavior.

  Reverting to the default behavior is always possible by upgrading with the

  rmiiclk_default.suf file.

  The lif,identification user command will reflect which file has been loaded.
- The PHY address is 001.

3 Supported Ethernet PHY's

The supported Ethernet PHY's can be found in the following table. The support is conditional to the firmware version and specifically:

- AsteRx-m3 should be running firmware 4.10.0 or higher
- AsteRx-i3 should be running firmware 1.3.1 or higher

If a PHY is not listed in the table, it is not supported.

Component	Supported Suffix	REF_CLK direction	rmiiclk_from_mac needed	Comment
KSZ8001	L, LI, S, SI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/REF_CLK
KSZ8021	RNL, RNLI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/REF_CLK
KSZ8031	RNL, RNLI	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REF_CLK, Note: PHY also needs 25 MHz on PHY/XI
KSZ8041	NLI, NLU, NLAM	MAC to PHY	No	Connect MAC/REF_CLK to PHY/REF_CLK
	RNL, RNLI, RNLAM	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REF_CLK, Note: PHY also needs 25 MHz on PHY/XI
	LL, LLI, TL, TLI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/REF_CLK
KSZ8051	RNLU, RNLUB, RNLV	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REF_CLK, Note: PHY also needs 25 MHz on PHY/XI
KSZ8061	RNBI, RNBV, RNBW	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REF_CLK, Note: PHY also needs 25 MHz on PHY/XI
	RNDI, RNDV, RNDW	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/XI
KSZ8081	RNDCA, RNDIA	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/XI
KSZ8091	RNBCA, RNBIA	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REF_CLK, Note: PHY also needs 25 MHz on PHY/XI
	RNACA, RNAIA	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REF_CLK, Note: PHY also needs 25 MHz on PHY/XI
	RNDCA, RNDIA	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/XI
KSZ8721	CL	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/REF_CLK
	BL, BLI, SL, SLI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/REF_CLK
	B, BT, BI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/REF_CLK

KSZ8863	RRL, RRLI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/X1 and/or PHY/REFCLKI_3 (configured with pin strapping)
		PHY to MAC	No	Connect MAC/REF_CLK to PHY/REFCLKO_3 (configured with pin strapping)
KSZ8864	RMNC, RMNI	MAC to PHY	Yes	Not documented here, contact us
	RMNUB	PHY to MAC	No	Not documented here, contact us
KSZ8873	RLL, RLLI	MAC to PHY	Yes	Connect MAC/REF_CLK to PHY/X1 and/or PHY/REFCLKI_3 (configured with pin strapping)
	RLLU, RLLAM	PHY to MAC	No	Connect MAC/REF_CLK to PHY/REFCLKO_3 (configured with pin strapping)

END OF DOCUMENT